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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/852,683	Applicant(s) ADACHI, KAORU	
	Examiner Christopher E. Lee	Art Unit 2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04 January 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-4 and 6-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 19-23 is/are allowed.
- 6) ☒ Claim(s) 1-4 and 6-18 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Receipt Acknowledgement

1. Receipt is acknowledged of the Amendment filed on 4th of January 2005. Claim 10 has been amended: no claim has been canceled; and claims 19-23 have been newly added since the RCE Non-Final Office Action was mailed on 6th of October 2004. Currently, claims 1-4 and 6-23 are pending in this application.

Claim Rejections - 35 USC § 103

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1, 6 and 10-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nozuyama [US 5,862,359 A] in view of Nakajima et al. [JP 2000020459 A; hereinafter Nakajima] and Kelley et al. [US 6,134,621 A; hereinafter Kelley].

Referring to claim 1, Nozuyama discloses an integrated circuit (i.e., LSI 10 of Fig. 1) in which a plurality of devices (i.e., functional blocks 11-20 in Fig. 3) and a control circuit (e.g., CPU 11 of Fig. 1) for controlling transfers of data with said devices (See col. 3, lines 18-23), wherein these devices are connected by a common bus (i.e., divisional busses 21-23, 232 and 233 in Fig. 3), said integrated circuit comprising: a plurality of switch circuits (i.e., bus switches 3 and 3a in Fig. 3), each for performing control to turn on and off (i.e., connection/disconnection) said bus connection between one device and another device (See col. 3, lines 29-41 and col. 6, lines 9-39); and at least one switch control circuit (i.e., decoders 4 and 4a in Fig. 3) for controlling said switch circuits (See col. 2, lines 21-25).

Nozuyama does not expressly teach said plurality of devices comprising a device for high-speed access, and two or more devices for lower-speed access in said integrated circuit and said control circuit for controlling in such a manner that transfers of data with said device for high-speed access takes priority over data transfers with said devices for lower-speed access, each of said switching circuit for performing

said control to turn on and off said bus connection between said device for high-speed access and a corresponding one of said devices for lower-speed access; and said at least one switch control circuit for controlling said switch circuits so as to turn off said bus connection between said device for high-speed access and each of said devices for lower-speed access when data is transferred to said device for high-speed access, and turn on said bus connection between said device for high-speed access and at least one of said devices for lower-speed access when data is transferred to at least one of said devices for lower-speed access.

Nakajima discloses a quick access control system for CPU (See Abstract), wherein a plurality of devices (i.e., CPU 1, FROM 2a, SRAM 2b, I/O 3a and LAP-B 3b in Fig. 1) comprising a device for high-speed access (e.g., SRAM 2b of Rapid Access Field 2 in Fig. 1), and two devices for lower-speed access (e.g., I/O 3a and LAP-B 3b in Fig. 1) in an integrated circuit (i.e., electronic instrument in Fig. 1) and a control circuit (i.e., bus control section 6 of Fig. 1) for controlling transfer of data to these devices (See Solution in Abstract) are connected by a common bus (i.e., data bus 4 of Fig. 1) in such a manner that transfer of data to said device for high-speed access (i.e., SRAM 2b of Fig. 1) takes priority over data transfers with said devices for lower-speed access (See col. 5, lines 16-20 and col. 6, line 39 through col. 7, line 1; i.e., wherein in fact that if the access instructions to which access operation to the rapid access field from the CPU is urged are detected, it constitutes from the bus control section which carries out change control of the bus switch so that the data bus between the usual access field may usually be carried out to the CPU at OFF implies that said common bus operates in such a manner that transfer of data to said device for high-speed access takes priority over data transfers with said devices for lower-speed access), a switching circuit (i.e., bus switch 5 of Fig. 1) for performing control to turn on and off (i.e., ON/OFF) said bus connection between said device for high-speed access and a corresponding one of said devices for lower-speed access (See col. 6, line 39 through col. 7, line 32); and a switch control circuit (i.e., bus control section 6 of Fig. 1) for controlling said switch circuit so as to turn off said bus connection between said

device for high-speed access and each of said devices for lower-speed access (e.g., between SRAM 2b of Rapid Access Field 2 and LAP-B 3b of Usual Access Field 3 in Fig. 1) when data is transferred to said device for high-speed access (See col. 6, line 47 through col. 7, line 1), and turn on said bus connection between said device for high-speed access and at least one of said devices for lower-speed access (i.e.,
5 between SRAM 2b of Rapid Access Field 2 and LAP-B 3b of Usual Access Field 3 in Fig. 1) when data is transferred to at least one of said devices for lower-speed access (See col. 6, lines 39-47).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said quick access control mechanism, as disclosed by Nakajima, in said integrated circuit, as disclosed by Nozuyama, for the advantage of offering a rapid access control system of said
10 high-speed access device (i.e., CPU) which realizes smooth rapid access among the rapid access fields for said high-speed access devices (See Nakajima, col. 3, lines 28-31).

Nozuyama, as modified by Nakajima, does not expressly teach said device for high-speed access, said devices for lower-speed access and said switch control circuit each operates in synchronization with common clock pulses, said common clock pulses having a period that varies based on said access speed
15 of said device to be accessed.

Kelley discloses a variable slot configuration for multi-speed bus (See Abstract), wherein a device for high-speed access (i.e., 66 MHz card), a device for low-speed access (i.e., 33 MHz card) and a switch control circuit (i.e., frequency control logic 121 of Fig. 1) each operates in synchronization with common clock pulses (i.e., clock 112 from clock control 66/33 MHz 111 in Fig. 1; See col. 2, lines 15-21), said
20 common clock pulses having a period that varies (i.e., clock periods for 33 MHz or 66MHz) based on said access speed of said device to be accessed (i.e., based on access 66MHz card or 33 MHz card; See Fig. 3).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said common clock pulses control, as disclosed by Kelly, in said integrated circuit, as disclosed by Nozuyama, as modified by Nakajima, for the advantage of providing mechanism to drive

said high-speed access device and said low-speed access device (i.e., 33 MHz card and 66 MHz card) in synchronization with said low-speed clock pulses (i.e., 33 MHz; See Kelly, col. 1, lines 22-41).

Referring to claim 6, Nozuyama discloses a method of controlling an integrated circuit (i.e., a method of data transfer bus provided between a plurality of functional blocks inside LSI 10 of Fig. 1; See col. 1, lines 6-13) in which a plurality of devices (i.e., functional blocks 11-20 in Fig. 3) and a control circuit (e.g., CPU 11 of Fig. 1) for controlling transfer of data with said devices (See col. 3, lines 18-23), wherein these devices are connected by a common bus (i.e., divisional busses 21-23, 232 and 233 in Fig. 3), said method comprising: providing a plurality of switch circuits (i.e., providing bus switches 3 and 3a in Fig. 3), each for performing control to turn on and off (i.e., connection/disconnection) said bus connection between one device and another device (See col. 3, lines 29-41 and col. 6, lines 9-39); and controlling said switch circuits (See col. 2, lines 21-25).

Nozuyama does not expressly teach said plurality of devices comprising a device for high-speed access, and two or more devices for lower-speed access in said integrated circuit and said control circuit for controlling in such a manner that transfers of data with said device for high-speed access takes priority over data transfers with said devices for lower-speed access, each of said switching circuit for performing said control to turn on and off said bus connection between said device for high-speed access and a corresponding one of said devices for lower-speed access; and said controlling said switch circuits so as to turn off said bus connection between said device for high-speed access and each of said devices for lower-speed access when data is transferred to said device for high-speed access and turn on said bus connection between said device for high-speed access and at least one of said devices for lower-speed access when data is transferred to at least one of said devices for lower-speed access.

Nakajima discloses a method for quick accessing control system for CPU (See Abstract), wherein a plurality of devices (i.e., CPU 1, FROM 2a, SRAM 2b, I/O 3a and LAP-B 3b in Fig. 1) comprising a device for high-speed access (e.g., SRAM 2b of Rapid Access Field 2 in Fig. 1), and two devices for

lower-speed access (e.g., I/O 3a and LAP-B 3b in Fig. 1) in an integrated circuit (i.e., electronic instrument in Fig. 1) and a control circuit (i.e., bus control section 6 of Fig. 1) for controlling transfer of data to these devices (See Solution in Abstract) are connected by a common bus (i.e., data bus 4 of Fig. 1) in such a manner that transfer of data to said device for high-speed access (i.e., SRAM 2b of Fig. 1) takes priority over data transfers with said devices for lower-speed access (See col. 5, lines 16-20 and col. 6, line 39 through col. 7, line 1; i.e., wherein in fact that if the access instructions to which access operation to the rapid access field from the CPU is urged are detected, it constitutes from the bus control section which carries out change control of the bus switch so that the data bus between the usual access field may usually be carried out to the CPU at OFF implies that said common bus operates in such a manner that transfer of data to said device for high-speed access takes priority over data transfers with said devices for lower-speed access), a switching circuit (i.e., bus switch 5 of Fig. 1) for performing control to turn on and off (i.e., ON/OFF) said bus connection between said device for high-speed access and a corresponding one of said devices for lower-speed access (See col. 6, line 39 through col. 7, line 32); and a switch control circuit (i.e., bus control section 6 of Fig. 1) for controlling said switch circuit so as to turn off said bus connection between said device for high-speed access and each of said devices for lower-speed access (e.g., between SRAM 2b of Rapid Access Field 2 and LAP-B 3b of Usual Access Field 3 in Fig. 1) when data is transferred to said device for high-speed access (See col. 6, line 47 through col. 7, line 1), and turn on said bus connection between said device for high-speed access and at least one of said devices for lower-speed access (i.e., between SRAM 2b of Rapid Access Field 2 and LAP-B 3b of Usual Access Field 3 in Fig. 1) when data is transferred to at least one of said devices for lower-speed access (See col. 6, lines 39-47).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said quick access control mechanism, as disclosed by Nakajima, in said integrated

circuit, as disclosed by Nozuyama, for the advantage of offering a rapid access control system of said high-speed access device (i.e., CPU) which realizes smooth rapid access among the rapid access fields for said high-speed access devices (See Nakajima, col. 3, lines 28-31).

Nozuyama, as modified by Nakajima, does not expressly teach operating said device for high-speed access, said devices for lower-speed access and said switch control circuit in synchronization with common clock pulses, said common clock pulses having a period that varies based on said access speed of said device to be accessed.

Kelley discloses a method of a variable slot configuration for multi-speed bus (See Abstract), wherein operating a device for high-speed access (i.e., 66 MHz card), a device for low-speed access (i.e., 33 MHz card) and a switch control circuit (i.e., frequency control logic 121 of Fig. 1) each operates in synchronization with common clock pulses (i.e., clock 112 from clock control 66/33 MHz 111 in Fig. 1; See col. 2, lines 15-21), said common clock pulses having a period that varies (i.e., clock periods for 33 MHz or 66MHz) based on said access speed of said device to be accessed (i.e., based on access 66MHz card or 33 MHz card; See Fig. 3).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said method for common clock pulses control, as disclosed by Kelly, in said method of controlling said integrated circuit, as disclosed by Nozuyama, as modified by Nakajima, for the advantage of providing mechanism to drive said high-speed access device and said low-speed access device (i.e., 33 MHz card and 66 MHz card) in synchronization with said low-speed clock pulses (i.e., 33 MHz; See Kelly, col. 1, lines 22-41).

Referring to claim 10, Nozuyama discloses an integrated circuit (i.e., LSI 10 of Fig. 1) comprising: three or more devices (i.e., functional blocks 11-20 in Fig. 3); a processor (i.e., CPU 11 of Fig. 1) configured to control data transfers for each said devices (See col. 3, lines 18-23); and a bus (i.e., divisional busses 21-23, 232 and 233 in Fig. 3) operably connecting each of said devices to said processor

such that said data transfers are performed over said bus (See col. 3, lines 29-41), said bus including a switch for said devices (i.e., bus switches 3 and 3a for functional blocks 11-20 in Fig. 3), wherein each switch (e.g., bus switch 3 of Fig. 1) is configured to disable a bus connection (i.e., disconnection) between corresponding devices (i.e., corresponding functional blocks, e.g., functional blocks 13 and 14 in Fig. 1) and said processor (i.e., CPU 11 of Fig. 1; See col. 6, lines 9-39).

Nozuyama does not expressly teach said devices including a first device configured for high-speed access and at least two devices configured for lower-speed access relative to said first; and said bus including said switch for each of said lower-speed access devices, wherein each switch is configured to disable a bus connection between corresponding lower-speed access devices and said processor when a data transfer performed with high-speed access device.

Nakajima discloses a quick access control system for CPU (See Abstract), wherein a plurality of devices (i.e., CPU 1, FROM 2a, SRAM 2b, I/O 3a and LAP-B 3b in Fig. 1) including a first device configured for high-speed access (e.g., SRAM 2b of Rapid Access Field 2 in Fig. 1) and at least two devices (e.g., I/O 3a and LAP-B 3b in Fig. 1) configured for lower-speed access relative to said first (i.e., said I/O 3a and LAP-B 3b being located in Usual Access Field 3 in Fig. 1); and a bus (i.e., data bus 4 of Fig. 1) including a switch (i.e., bus switch 5 of Fig. 1) being configured to disable a bus connection (i.e., disconnection) between corresponding lower-speed access devices (i.e., I/O and LAP-B) and a processor (i.e., CPU 1 of Fig. 1) when a data transfer performed with high-speed access device (See col. 6, line 47 through col. 7, line 1).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said quick access control mechanism, as disclosed by Nakajima, in said integrated circuit, as disclosed by Nozuyama, for the advantage of offering a rapid access control system of said high-speed access device (i.e., CPU) which realizes smooth rapid access among the rapid access fields for said high-speed access devices (See Nakajima, col. 3, lines 28-31).

Nozuyama, as modified by Nakajima, does not expressly teach said three or more devices being configured to operate in synchronization with a common clock signal, wherein a period of said common clock signal varies based on an access speed of said device associated with said data transfer being performed over said bus.

- 5 Kelly discloses a variable slot configuration for multi-speed bus (See Abstract), wherein three or more devices (e.g., 66 MHz cards and 33 MHz cards on SLOT#1-4 117, 119, 127 and 129 in Fig. 1) being configured to operate in synchronization with a common clock signal (i.e., clock 112 from clock control 66/33 MHz 111 in Fig. 1; See col. 2, lines 15-21), wherein a period of said common clock signal varies (i.e., clock periods for 33 MHz or 66MHz) based on an access speed of said device associated with said data transfer being performed over said bus (i.e., based on access 66MHz card or 33 MHz card over PCI bus 115 in Fig. 1; See Fig. 3).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said common clock pulses control, as disclosed by Kelly, in said integrated circuit, as disclosed by Nozuyama, as modified by Nakajima, for the advantage of providing mechanism to drive said high-speed access device and said low-speed access device (i.e., 33 MHz card and 66 MHz card) in synchronization with said low-speed clock pulses (i.e., 33 MHz; See Kelly, col. 1, lines 22-41).

Referring to claim 11, Nakajima teaches a switch controller (i.e., bus control section 6 of Fig. 1) configured to control said switch (i.e., bus switch 5 of Fig. 1) to disable said bus connection (i.e., disconnection) to said corresponding lower-access speed device (e.g., LAP-B 3b of Usual Access Field 3 in Fig. 1) when a data transfer is being performed with said first device (e.g., SRAM 2b of Rapid Access Field 2 in Fig. 1; See col. 6, line 47 through col. 7, line 1), and to enable said bus connection (i.e., connection) to said corresponding lower-access speed device (i.e., LAP-B 3b of Usual Access Field 3 in Fig. 1) when a data transfer is being performed with said corresponding lower-access speed device (See col. 6, lines 39-47).

Referring to claim 12, Nozuyama teaches each switch (i.e., bus switches 3 and 3a in Fig. 3) comprising a metal oxide semiconductor (i.e., CMOS switch circuit; See col. 6, lines 1-8) connected to said bus (i.e., divisional busses 21-23, 232 and 233 in Fig. 3).

Referring to claim 13, Nozuyama, as modified by Nakajima and Kelly, teaches all the limitations of the claim 13, such that Nakajima teaches said lower-speed access devices (i.e., devices in Usual Access Field 3 in Fig. 1) including second and third devices (i.e., I/O 3a and LAP-B 3b in Fig. 1), and Nozuyama teaches a first portion of said bus (i.e., divisional bus 21 in Fig. 3) operably connects said first device (e.g., functional block (ROM) 12 of Fig. 3) to said processor (e.g., functional block (CPU) 11 of Fig. 3), a second portion of said bus (i.e., divisional bus 23 in Fig. 3) operably connects (i.e., by the operation of bus switch 3 in Fig. 3) said second device (e.g., functional blocks 15 and 16 in Fig. 3) to said first portion of said bus (i.e., divisional bus 21 in Fig. 3), and a third portion of said bus (i.e., divisional bus 232 in Fig. 3) connects (i.e., by the operation of bus switch 3a in Fig. 3) said third device (e.g., functional blocks 17 and 18 in Fig. 3) to said second portion of said bus (i.e., divisional bus 23 in Fig. 3), and said switch (i.e., bus switch 3 of Fig. 3) for said second device is configured to selectively enable and disable said second portion of said bus (See col. 3, lines 13-17), and said switch for said third device is configured to selectively enable and disable said third portion of said bus (See col. 6, lines 50-61).

Referring to claim 14, Nozuyama, as modified by Nakajima and Kelly, teaches said second device (i.e., functional blocks 15 and 16 in Fig. 3; Nozuyama) is configured for higher-speed access than said third device (i.e., functional blocks 17 and 18 in Fig. 3; Nozuyama). See Nakajima, col. 3, lines 16-27, and Nozuyama, col. 3, lines 29-53, for the suggestion of said high-speed access (i.e., high frequency operation) and said lower-speed access (viz., lower frequency operation) configuration.

Referring to claim 15, Nozuyama teaches at least one switch controller (i.e., decoders 4 and 4a in Fig. 3) configured to: control said switch (i.e., bus switch 3 of Fig. 3) for said second device (i.e., functional blocks 15 and 16 in Fig. 3) to disable said second portion of said bus (i.e., disconnect) when a

data transfer is being performed with said first device (i.e., functional blocks 11 and 12 in Fig. 3; e.g., when a data transfer is performed between functional block (CPU) 11 and functional block (ROM) 12 in Fig. 3), and to enable said second portion of said bus (i.e., connect) when a data transfer is being performed with said second device (i.e., functional blocks 15 and 16 in Fig. 3; e.g., when a data transfer is performed between functional block (CPU) 11 and functional block 15 in Fig. 3); and control said switch for third device (i.e., functional blocks 17 and 18 in Fig. 3) disable said third portion of said bus (i.e., disconnection) when a data transfer is being performed with said second device (i.e., functional blocks 15 and 16 in Fig. 3; e.g., when a data transfer is performed between functional block (CPU) 11 and functional block 15 in Fig. 3), and to enable said third portion of said bus (i.e., connect) when a data transfer is being performed with said third device (i.e., functional blocks 17 and 18 in Fig. 3; e.g., when a data transfer is performed between functional block (CPU) 11 and functional block 17 in Fig. 3).

Referring to claim 16, Nozuyama teaches said at least one switch controller (i.e., decoders in Fig. 3) comprises a plurality of switch controllers (i.e., decoders 4 and 4a in Fig. 3), one of said switch controllers (e.g., decoder 4 of Fig. 3) being configured to control said switch for said second device (i.e., decoder 4 controlling bus switch 3 for functional blocks 15 and 16 in Fig. 3), and another one of said switch controllers (e.g., decoder 4a of Fig. 3) being configured to control said switch for said third device (i.e., decoder 4a controlling bus switch 3a for functional blocks 17 and 18 in Fig. 3).

Referring to claim 17, Nozuyama teaches said switch (i.e., bus switch 3 of Fig. 3) for said second device (i.e., functional block 15 and 16 in Fig. 3) comprises a metal oxide semiconductor (i.e., CMOS switch circuit; See col. 6, lines 1-8) connected to said second portion of said bus (i.e., divisional bus 23 in Fig. 3), and said switch (i.e., bus switch 3a of Fig. 3) for said third device (i.e., functional block 17 and 18 in Fig. 3) comprises a MOS (i.e., said CMOS switch circuit) connected to said third portion of said bus (i.e., divisional bus 232 in Fig. 3).

Referring to claim 18, Nozuyama teaches said devices (i.e., functional blocks 11-20 in Fig. 3) are connected at respective points of said bus (See Fig. 3), such that said relative distances between said processor and said connection points of said devices increase as said operating speed of said respective devices decrease (See col. 3, lines 29-53; i.e., wherein in fact that the access frequency to a functional block connected to a divisional bus is defined in the unit of a pair of a functional block for outputting data to the divisional bus and a functional block for receiving data from the divisional bus implies that said relative distances between said processor and said connection points of said devices increase as said operating speed of said respective devices decrease).

4. Claims 2 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nozuyama [US 5,862,359 A] in view of Nakajima [JP 2000020459 A] and Kelley [US 6,134,621 A] as applied to claims 1, 6 and 10-18 above, and further in view of Cepulis et al. [US 6,061,754 A; hereinafter Cepulis].

Referring to claim 2, Nozuyama, as modified by Nakajima and Kelly, discloses all the limitations of the claim 2 including said device for high-speed access (i.e., FROM 2a, SRAM 2b of Rapid Access Field 2 in Fig. 1; Nakajima) and said devices for lower-speed access (i.e., I/O 3a and LAP-B 3b of Usual Access Field 3 in Fig. 1; Nakajima) are connected by said common bus (i.e., data bus 4 of Fig. 1; Nakajima) so as to be given priority for data transfer in order of decreasing access speed (See Nakajima, col. 7, lines 46-49; in fact, higher priority is given to a device in Rapid Access Field, e.g., SRAM 2b, by the bus switch and by the neighborhood of CPU); each of said switch circuits (i.e., each of bus switches 3 and 3a in Fig. 3; Nozuyama, and bus switch 5 in Fig. 1; Nakajima) being provided between mutually adjacent devices (i.e., between SRAM of Rapid Access Field and LAP-B of Usual Access Field; Nakajima) among said devices for high-speed access (i.e., devices for Rapid Access; Nakajima) and lower-speed access (i.e., devices for Usual Access; Nakajima) in order to turn on and off (i.e., connecting and cutting; Nakajima) said bus connection between said mutually adjacent devices among said plurality of devices (See Nakajima, col. 6, line 39 through col. 7, line 32), except that does not expressly teach said

switching control circuit controlling said switch circuits in sequence so as to turn on said respective bus connections so as to enable access to devices of higher access speed before enabling access to devices of lower access speed.

Cepulis discloses a data bus having switch for selectively connecting and disconnecting devices to or

5 from the bus (See Abstract and Fig. 8), wherein a device for high-speed access (e.g., Bus Agent 842 in Fig. 8) and devices for low-speed access (e.g., Bus Agents 843-846 in Fig. 8) are connected by a common bus (i.e., bus 810 of Fig. 8) so as to be given priority for data transfer in order of decreasing access speed (See col. 7, line 66 through col. 8, line 31); each of switch circuits (i.e., bus switches 851-854 in Fig. 8) being provided between mutually adjacent devices among said devices (i.e., said bus switches are located
10 between mutually adjacent Bus Agents 842-846 in Fig. 8) for high-speed access and lower-speed access (See col. 8, lines 27-31) in order to turn on and off (i.e., close and open) a bus connection between said mutually adjacent devices among said plurality of devices (i.e., closing/opening bus connections at bus switch 851, at bus switch 852, at bus switch 853 and at bus switch 854, See col. 6, line 39 through col. 7, line 32); a switch control circuit (i.e., means for controlling the state of the bus switch; See col. 2, line 57)
15 controlling said switch circuits (i.e., bus switches) in sequence so as to turn on said respective bus connections so as to enable access to devices of higher access speed having a higher access speed (See col. 2, lines 42-60) before enabling access to devices of lower access speed (See col. 7, line 66 through col. 8, line 31).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was
20 made to have inclusively expanded the function of said control circuit (i.e., decoder; Nozuyama) for controlling said switch circuit, as disclosed by Nozuyama, as modified by Nakajima and Kelly, to the function of said control circuit (i.e., means for controlling the state of the bus switch) for controlling said switch circuits (i.e., plural bus switches), as disclosed by Cepulis, for the advantage of providing an ability to maximize data transfer rates on the bus (See Cepulis, col. 3, lines 16-18).

Referring to claim 7, Nozuyama, as modified by Nakajima and Kelly, discloses all the limitations of the claim 7 including connecting said device for high-speed access (i.e., FROM 2a, SRAM 2b of Rapid Access Field 2 in Fig. 1; Nakajima) and said devices for lower-speed access (i.e., I/O 3a and LAP-B 3b of Usual Access Field 3 in Fig. 1; Nakajima) by said common bus (i.e., data bus 4 of Fig. 1; Nakajima) so as
5 give priority for data transfer to said connected devices in order of decreasing access speed (See Nakajima, col. 7, lines 46-49; in fact, higher priority is given to a device in Rapid Access Field, e.g., SRAM 2b, by the bus switch and by the neighborhood of CPU); providing each of said switch circuits (i.e., each of bus switches 3 and 3a in Fig. 3; Nozuyama, and bus switch 5 in Fig. 1; Nakajima) between mutually adjacent devices (i.e., between SRAM of Rapid Access Field and LAP-B of Usual Access Field;
10 Nakajima) among said devices for high-speed access (i.e., devices for Rapid Access; Nakajima) and lower-speed access (i.e., devices for Usual Access; Nakajima) in order to turn on and off (i.e., connecting and cutting; Nakajima) said bus connection between said mutually adjacent devices among said plurality of devices (See Nakajima, col. 6, line 39 through col. 7, line 32), except that does not expressly teach controlling said switch circuits in sequence so as to turn on said respective bus connections so as to enable
15 access to devices of higher access speed before enabling access to devices of lower access speed.

Cepulis discloses a data bus having switch for selectively connecting and disconnecting devices to or from the bus (See Abstract and Fig. 8), wherein connecting a device for high-speed access and devices for low-speed access (e.g., Bus Agent 842 being connected to Bus Agents 843-846 in Fig. 8) by a common bus (i.e., bus 810 of Fig. 8) so as to be given priority for data transfer in order of decreasing access speed
20 (See col. 7, line 66 through col. 8, line 31); providing each of switch circuits (i.e., bus switches 851-854 in Fig. 8) between mutually adjacent devices among said devices (i.e., said bus switches are located between mutually adjacent Bus Agents 842-846 in Fig. 8) for high-speed access and lower-speed access (See col. 8, lines 27-31) in order to turn on and off (i.e., close and open) a bus connection between said mutually adjacent devices among said plurality of devices (i.e., closing/opening bus connections at bus

switch 851, at bus switch 852, at bus switch 853 and at bus switch 854, See col. 6, line 39 through col. 7, line 32); controlling said switch circuits (i.e., bus switches) in sequence so as to turn on said respective bus connections so as to enable access to devices of higher access speed having a higher access speed (See col. 2, lines 42-60) before enabling access to devices of lower access speed (See col. 7, line 66 through col. 8, line 31).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have inclusively expanded the function of said control circuit (i.e., decoder; Nozuyama) for controlling said switch circuit, as disclosed by Nozuyama, as modified by Nakajima and Kelly, to the function of said control circuit (i.e., means for controlling the state of the bus switch) for controlling said switch circuits (i.e., plural bus switches), as disclosed by Cepulis, for the advantage of providing an ability to maximize data transfer rates on the bus (See Cepulis, col. 3, lines 16-18).

5. Claims 3, 4, 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nozuyama [US 5,862,359 A] in view of Nakajima [JP 2000020459 A] and Kelley [US 6,134,621 A] as applied to claims 1, 6 and 10-18 above, and further in view of Tsukamoto [US 3,594,656].

Referring to claim 3, Nozuyama, as modified by Nakajima and Kelly, discloses all the limitations of the claim 3 including said switch control circuit (i.e., bus control section 8 of Fig. 1; Nakajima) controls each of said switch circuits (i.e., each of bus switches 3 and 3a in Fig. 3; Nozuyama, and bus switch 5 in Fig. 1; Nakajima) so as to turn on said bus connection (See Fig. 1; Nakajima), except that does not expressly teach said control circuit being configured to output, in sync with said common clock pulses, a data-transfer enable signal that enables transfer of data upon elapse of a fixed period of time after said switch control circuit controls each of said switch circuits so as to turn on said bus connection. Tsukamoto discloses an automatic clock frequency-switching system (See Fig. 1 and Abstract), wherein a control circuit (i.e., clock frequency control 16 of Fig. 1) is configured to output, in sync with common clock pulses (i.e., clock signal), a data-transfer enable signal (i.e., frequency-switching signal via line 19c

in Fig. 1) that enables transfer of data (See col. 2, lines 68-72) upon elapse of a fixed period of time (i.e., predetermined time has been elapsed; See col. 4, lines 43-51) after a switch control circuit (i.e., clock frequency control 19 of Fig. 1) controls a switch circuit (i.e., frequency selector 12 of Fig. 1; See col. 2, lines 63-68).

5 Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said automatic clock frequency-switching system, as disclosed by Tsukamoto, in said integrated circuit, as disclosed by Nozuyama, as modified by Nakajima and Kelly, so as said changed common clock to be effected upon elapse of a fixed period of time (i.e., predetermined time) after said control circuit controls said switch circuit so as to turn on said bus connection for the advantage of
10 obviating any drawbacks caused by a variation of frequency over a wide range (See Tsukamoto, col. 1, lines 42-57).

Referring to claim 8, Nozuyama, as modified by Nakajima and Kelly, discloses all the limitations of the claim 8 including controlling each of said switch circuits (i.e., each of bus switches 3 and 3a in Fig. 3; Nozuyama, and bus switch 5 in Fig. 1; Nakajima) to turn on said bus connection (See Fig. 1;
15 Nakajima), except that does not expressly teach outputting, in sync with said common clock pulses, a data-transfer enable signal that enables transfer of data upon a fixed period of time elapsing after controlling each of said switch circuits to turn on said bus connection.

Tsukamoto discloses an automatic clock frequency-switching system (See Fig. 1 and Abstract), wherein outputting (i.e., a control circuit being configured to output clock frequency control 16 in Fig. 1), in sync
20 with common clock pulses (i.e., clock signal), a data-transfer enable signal (i.e., frequency-switching signal via line 19c in Fig. 1) that enables transfer of data (See col. 2, lines 68-72) upon a fixed period of time elapsing (i.e., predetermined time has been elapsed; See col. 4, lines 43-51) after controlling controls a switch circuit (i.e., clock frequency control 19 controls frequency selector 12 in Fig. 1; See col. 2, lines 63-68).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said automatic clock frequency-switching system, as disclosed by Tsukamoto, in said integrated circuit, as disclosed by Nozuyama, as modified by Nakajima and Kelly, so as said changed common clock to be effected upon elapse of a fixed period of time (i.e., predetermined time) after said control circuit controls said switch circuit so as to turn on said bus connection for the advantage of obviating any drawbacks caused by a variation of frequency over a wide range (See Tsukamoto, col. 1, lines 42-57).

Referring to claims 4 and 9, Tsukamoto teaches output timing (i.e., T_e in Fig. 2) said data-transfer enable signal (i.e., frequency-switching end signal 19c in Fig. 2) output from said output circuit (i.e., clock frequency control 19 of Fig. 2) differs in dependence upon said access speeds of said devices (in fact, said output timing T_e is differing in dependence upon a new clock speed in α and β phases because the predetermined time is consisted of T_b and T_c , which are in time dependence upon said newly changed clock speed in α and β phases in Fig. 2).

Allowable Subject Matter

6. Claims 19-23 are allowed.

7. The following is a statement of reasons for the indication of allowable subject matter:

With respect to claim 19, the claim limitations are deemed allowable over the prior art of record as the prior art fails to teach or suggest that data transfer on the bus starts when the bus start signal is enabled and the data complete signal is disabled, wherein a delay between enabling of the bus start signal and disabling of the data complete signal varies based on enabled/disabled states of the first and second switches. The claims 20-23 are dependent claims of the claim 19.

Response to Arguments

8. Applicant's arguments filed on 4th of January 2005 have been fully considered but they are not persuasive.

In response to the Applicant's argument with respect to "... In this instance, Nozuyama teaches away from Nakajima as well as away from the claimed invention. ... The primary objective of Nozuyama is to provide low power consumption data transfer bus such as a bus that is used in a micro-processor, a micro-controller or the bus provided between large scale integrated like. ... Clearly, in this example, there

5 *is no guarantee of any speed differential between the pairwise function blocks 11 and to that of pairwise function blocks 13 and 14."* on the Response page 13, line 15 through page 16, line 22, the Examiner respectfully disagrees.

First of all, the Applicant essentially argues that Nozuyama reference relied on in a rejection is inapplicable or cannot be combined because it does not relate to solving the same problem that the

10 Applicant is addressing in its claimed invention (i.e., NOT the object of the claimed invention). The motivation to do what the Applicant has done, however, does not have to be the same as the Applicant's to reach a conclusion of obviousness (See MPEP 2144). Moreover, the obviousness is not determined on the basis of purpose alone. *In re Graf*, 343 F.2d 774, 777, 145 USPQ 197, 199 (CCPA 1965). In summary, as long as there is some suggestion/motivation within the prior art to make the modification or

15 combination, it does not have to be the same as the Applicant's.

Secondly, Nozuyama discloses not only the concerning of achieving the low power consumption on LSI chip or LSI mounted board (See Abstract), but also the concerning of relating to the access frequency of a divisional bus (See col. 3, lines 55+). Nozuyama clearly states the motivation of the invention, such that without the mode of the division of the bus (i.e., without using a bus switch circuit), the achievement of

20 the low power consumption is not completely realized, and the operation speed of the bus (i.e., bus access frequency) is decreased as compared to the case where the bus is not divided by the bus switch circuit (See col. 2, lines 2-5).

At last, Nakajima discloses a quick access control system for CPU by controlling a bus switch for a data bus (See Abstract), which is very similar to the object of the Applicant's claimed invention.

As a result, Nozuyama and Nakajima do not teach away from the claimed invention, and thus the Applicant's argument on this point is not persuasive.

In response to the Applicant's argument with respect to "In contrast, the Examiner asserts that Nakajima discloses a plurality of devices configured for high speed access and low speed access. ... Even assuming the Examiner's assertions are taken to be true, this is in clear contrast to the teachings of Nozuyama which require no such division of speed differentials across the switches. Indeed, Nozuyama actually teaches away from Nakajima as asserted. Therefore, Nozuyama and Nakajima cannot be properly combined." on the Response page 17, lines 1-15, the Examiner respectfully disagrees.

In contrary to the Applicant's assertion, Nozuyama and Nakajima do not teach away from the claimed invention, which had been discussed in the above argument response.

Moreover, Nozuyama concerns the access frequency of a divisional bus. In other words, Nozuyama requires bus division of bus access speed (e.g., access frequency of a divisional bus of a smaller number is higher than the access frequency of a divisional bus of a larger number) across the bus switch circuit (See col. 3, lines 55+).

Thus, the Applicant's argument on this point is not persuasive.

In response to the Applicant's argument with respect to "Further, combining Nozuyama with Nakajima would render each other's device unsatisfactory for its intended purpose. For example, modifying Nozuyama by the asserted teachings Nakajima would not achieve the goal of minimizing power consumption of the LSI device. This clearly renders Nozuyama unsatisfactory for its intended purpose." on the Response page 17, lines 16-21, the Examiner respectfully disagrees.

In fact, Nozuyama discloses not only the concerning of achieving the low power consumption on LSI chip or LSI mounted board (See Abstract), but also the concerning of relating to the access frequency of a divisional bus (See Nozuyama, col. 3, lines 55+). Therefore, the combination of Nozuyama and Nakajima suggests the obviousness of the claimed invention with rationale for the combination, which offers a rapid

access control system of said high-speed access device which realizes smooth rapid access among the rapid access fields for said high-speed access devices (See Nakajima, col. 3, lines 28-31). It would not render each other's device unsatisfactory for its intended purpose.

Thus, the Applicant's argument on this point is not persuasive.

5 *In response to the Applicant's arguments with respect to § 103 REJECTION-NOZUYAMA, NAKAJIMA, KELLEY, CEPULIS on the Response page 18, line 6 through page 19, line 3, and § 103 REJECTION-NOZUYAMA, NAKAJIMA, KELLEY, TSUKAMOTO on the Response page 19, lines 4-21, the Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language*
10 *of the claims patentably distinguishes them from the references. In other words, the Applicant does not specify how the language of the claims 2-9 patentably distinguishes them from the references, especially Kelley, Cepulis, and/or Tsukamoto.*

Thus, the Applicant's arguments on these points are not persuasive.

Conclusion

15 9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
Wertheim et al. [US 6,662,260 B1] disclose electronic circuits with dynamic bus partitioning.
Yee et al. [US 5,491,814 A] disclose apparatus using a state machine for generating selectable clock frequencies and a fixed frequency for operating a computer bus.
Kelley et al. [US 6,295,568 B1] disclose method and system for supporting multiple local buses
20 operating at different frequencies.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

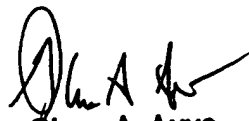
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 571-272-3637. The examiner can normally be reached on 9:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christopher E. Lee
Examiner
Art Unit 2112

cel/ *CEL*


Glenn A. Auve
Primary Patent Examiner
Technology Center 2100